GaAs Nonlinear Transmission Lines for Picosecond Pulse Generation and Millimeter-Wave Sampling

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***Abstract*—The GaAs nonlinear transmission line (NLTL) is a monolithic millimeter-wave integrated circuit consisting of a high-impedance transmission line loaded by reverse-biased Schottky contacts. Through generation of shock waves on the NLTL, we have generated electrical step functions with ~5 V magnitude and less than 1.4 ps fall time. Diode sampling bridges strobed by NLTL shock-wave generators have attained bandwidths approaching 300 GHz and have applications in instruments for millimeter-wave waveform and network measurements. We discuss the circuit design and diode design requirements for picosecond NLTL shock-wave generators and NLTL-driven sampling circuits.**

I. INTRODUCTION

WITH recent work in the GaAs/AlGaAs, InGaAs/AlGaAs/GaAs, and AlInAs/GaInAs/InP material systems [1], transistor cutoff frequencies have approached 350 GHz, and 100 GHz [2] monolithic millimeter-wave integrated circuits (MIMIC's) have been reported. Both the transistors and the MIMICs have developed more rapidly than the instrumentation used to characterize them.

In millimeter-wave transistor work, dc–65 GHz network measurements are extrapolated, yielding estimated 100–350 GHz $f_{\max}$. There is significant uncertainty in the extrapolation of power gain and of the circuit model, impairing physical understanding. In MIMIC design above 65 GHz, an extrapolated device model must be used, and the circuit design will show poor correlation with the measured MIMIC performance. Further, while device models can be extrapolated, circuit measurements cannot.

Sampling oscilloscopes and microwave network analyzers use diode sampling bridges to down-convert the signal under test to a lower frequency before acquisition. The instrument bandwidth is limited by the sampling circuit bandwidth, which in turn is limited by sampling diode parasitics and by the duration of the strobe pulse used to gate the sampling diodes into forward conduction. Since 1966 [3], step-recovery diodes (SRD's) [4] have been used for strobe pulse generation [5], [6], and the attainable ~25–30 ps SRD pulse widths have limited sampling circuit bandwidth to ~15–30 GHz. The nonlinear transmission line (NLTL) generates step functions more than 15 times faster than SRD's, allowing instrument bandwidths approaching 300 GHz.

While submicron lithography and advanced materials are variously required to attain 200–350 GHz transistor $f_{\max}$, 2–3 THz Schottky diodes can be easily fabricated with 3-mask processes, large 2–3 μm device dimensions, and simple GaAs material technologies [7], [8]. The circuits which can be implemented with such diodes will attain far larger bandwidths than circuits using 350 GHz transistors. Using nonlinear wave propagation effects [9]–[14] on nonlinear transmission lines, the Schottky diode can be used for impulse or step-function compression. The speed of such circuits is limited by the diode cutoff frequency, and picosecond pulses can be generated. Because sampling bridges and NLTL's require the same circuit elements, monolithic millimeter-wave sampling circuits using NLTL strobe pulse generators can be fabricated which attain bandwidths much greater than SRD-gated circuits [19]–[21].

II. THE NONLINEAR TRANSMISSION LINE

The GaAs nonlinear transmission line (Fig. 1(a)) is an MIMIC consisting of a high-impedance line of impedance Z_l loaded at spacings d (spacings of $\tau = d/v_{\mathrm{cpw}}$ in units of time delay) by reverse-biased Schottky contacts serving as voltage-variable capacitors. Here v_{cpw} is the propagation velocity of the high-impedance coplanar waveguide (CPW) line sections. Fig. 1(b) shows the approximate equivalent circuit, where

$$L = Z_l \tau \quad \text{and} \quad C_l = \tau / Z_l \tag{1}$$

are the line section inductance and capacitance, and

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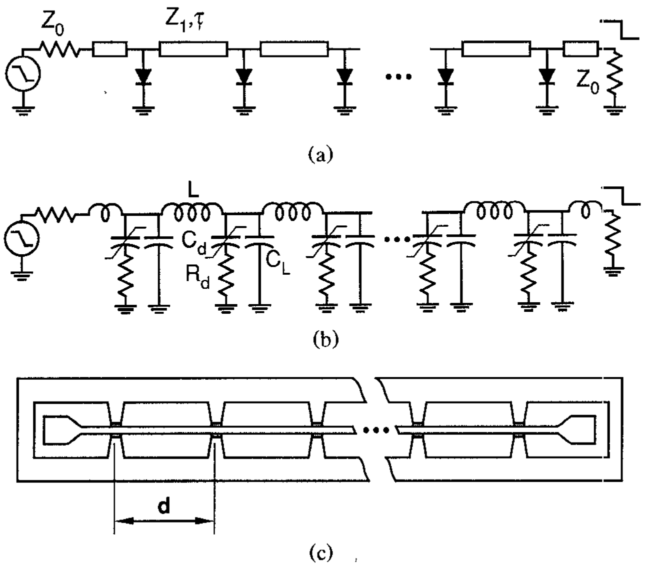


Fig. 1. (a) Circuit diagram, (b) equivalent circuit, and (c) layout of nonlinear transmission line.

$C_d(V)$ and R_d are the diode capacitance and parasitic series resistance. The diode (small-signal) cutoff frequency is $\omega_d = 1/C_d(V)R_d$ at bias voltage V. NLTL's are most readily implemented using coplanar waveguide lines (Fig. 1(c)).

The NLTL is a nonlinear, dispersive, and lossy network. Frequency-dependent losses arise both from R_d and skin-effect losses. The periodic structure is an undesired low-pass filter with a cutoff (Bragg) frequency of $\omega_{\text{per}} = 2/\sqrt{L(C_l + C_d(V))}$ and strong group-delay dispersion for $\omega \approx \omega_{\text{per}}$. The variable diode capacitance introduces a desired reduction in propagation delay with increasing reverse bias, resulting in the reduction of the fall time of waves propagating on the NLTL.

Our work, engineering of functional monolithic NLTL's, draws heavily on extensive analyses by Landauer [9], [22]–[24] and others [10]–[12], [14], [25]. We will restate (without proof) needed results from the literature in terms of GaAs monolithic structures.

A. Shock Wave Formation

Wavefront evolution during the compression phase, necessary NLTL length for wavefront compression, and the NLTL characteristic impedance can all be predicted neglecting ω_d and ω_{per}.

First consider an idealized nonlinear transmission line where $R_d = 0$ and ω_{per} is made very large by simultaneously reducing both the diode spacings, d, and the diode capacitances, $C_d(V)$, such that the diode capacitance per unit length, $C_d(V)/d$, remains constant. In this limit of a nearly continuous line [22], the voltage at the nth diode is

$$V_n(t) = V_{\text{in}}(t - nT(V)) \tag{2}$$

where

$$T(V) = \sqrt{LC_T(V)} \tag{3}$$

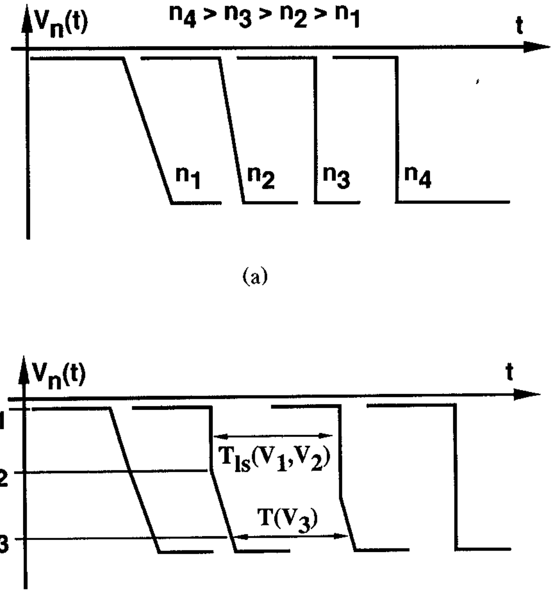


Fig. 2. (a) NLTL wavefront compression with step-function input. (b) Wavefront evolution caused by differing propagation delays of shock wave and remaining waveform.

is the propagation delay and $C_T(V) = C_d(V) + C_l$ is the total capacitance per NLTL section. The variation in propagation delay, $T(V)$, results in the compression of negative-going wavefronts during propagation. As an input signal $V_{\text{in}}(t)$, a falling step function with initial voltage V_h, final voltage V_l, and (input) fall time $T_{f,\text{in}}$ propagates on the line, the fall time $T_{f,n}$ at the nth NLTL section will at first decrease linearly with distance (Fig. 2(a)):

$$T_{f,n} = T_{f,\text{in}} - n\,\Delta T = T_{f,\text{in}} - n(T(V_h) - T(V_l)) \tag{4}$$

where ΔT is the fall time compression per NLTL section.

After a sufficient number of NLTL sections, (2) and (4) predict that the fall time will become less than zero. At this point, the voltage $V_n(t)$ becomes discontinuous, forming a shock wave, and (2) and (4) apply only to the *continuous portions* of $V_n(t)$ outside of the shock wavefront. With large ω_d and ω_{per}, the number of NLTL sections necessary to form a shock wave is $n = T_{f,\text{in}}/\Delta T$.

B. Shock Wave Propagation

Shock waves have propagation properties determined by the average or large-signal diode capacitance C_{ls}:

$$C_{ls}(V_l, V_h) = \frac{1}{V_h - V_l}\int_{V_l}^{V_h} C_d(V)\,dV. \tag{5}$$

After formation, the shock wave will have a propagation delay per NLTL section of [22]

$$T_{ls}(V_l, V_h) = \sqrt{L_l(C_{ls}(V_l, V_h) + C_l)}\,. \tag{6}$$

Unless $V_{\text{in}}(t)$ has the same time variation of voltage as $T(V)$ (eq. (3)), the shock wave will not form simultaneously over the full waveform amplitude, but instead will first form as a partial-amplitude shock wave whose amplitude is a fraction of total signal voltage (Fig. 2(b)). The partial shock of Fig. 2(b) between V_1 and V_2 will have a per-section propagation delay of $T_{ls}(V_1, V_2)$, while the more negative voltages in the vicinity of V_3 have a smaller propagation delay $T(V_3)$, and the point of the waveform at voltage V_3 will thus eventually join the shock wavefront. The partial shock amplitude will grow with propagation, and a shock wave of full amplitude is eventually formed.

The variation in $C_d(V)$ introduces a voltage variation in the small-signal characteristic impedance $Z_0(V) = \sqrt{L/(C_l + C_d(V))}$. For step functions propagating on the NLTL after shock formation, the voltage and current I_n are related by a constant large-signal wave impedance Z_{ls} [24], [18], $I_n(t) = I_{\rm dc} + V_n(t)/Z_{ls}(V_l, V_h)$, where

$$Z_{ls}(V_l, V_h) = \sqrt{\frac{L}{C_L + C_{ls}(V_l, V_h)}}. \qquad (7)$$

Shock waves are propagated *without reflection or distortion* from the NLTL to the load if $Z_{ls}(V_l, V_h) = Z_{\rm load}$.

C. Fall Time Limitations

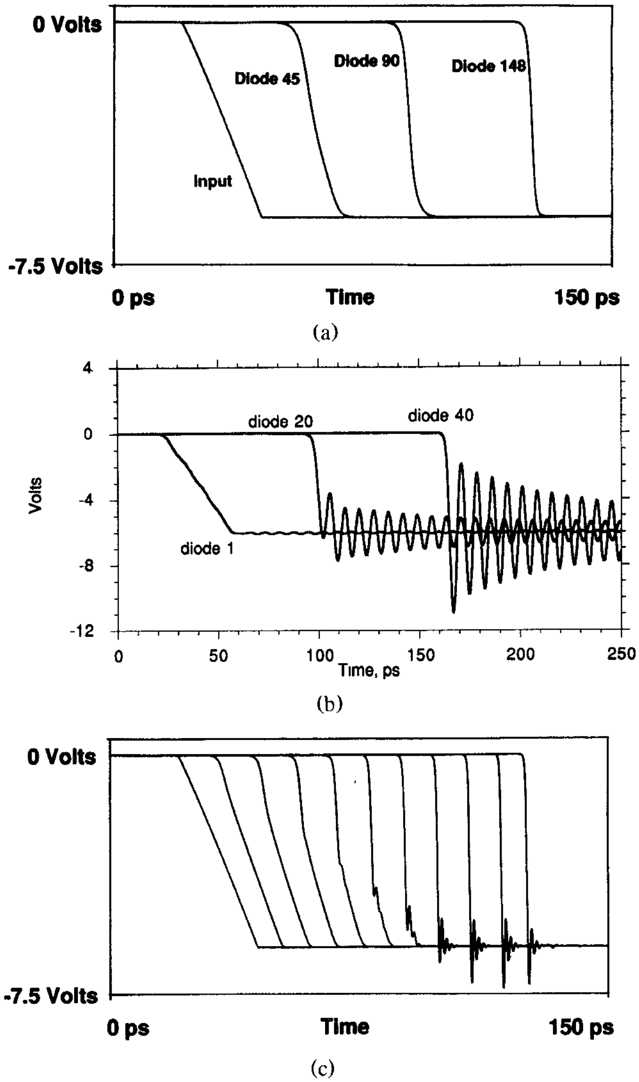
With nonzero $\omega_{\rm per}$ and ω_d the shock fall time will asymptotically approach a minimum compressed fall time, $T_{f,\min}$, at which wavefront compression ΔT is balanced by the wavefront spreading associated with $\omega_{\rm per}$ and ω_d.

If the diode cutoff frequency dominates $(\omega_d \sim\, < \omega_{\rm per})$, the minimum compressed fall time can be found analytically, assuming uniform Schottky diode doping [25], [18], [17]. In this case $C_d(V) = C_{j0}/\sqrt{1 + V/\phi}$, and

$$T_{f,\min}(10\% - 90\%) = \frac{8.8}{\omega_d(0)} \frac{1}{\sqrt{1 - V_l/\phi} - 1} \qquad (8)$$

assuming that $V_h = 0$ V. Given a typical GaAs Schottky diode with $\phi \approx 0.8$ V and $\omega_d(0)/2\pi \approx 1$ THz, (8) predicts a 0.73 ps fall time for a 6 V step-function input. For more general diode doping profiles, $T_{f,\min} \propto 1/\omega_d$ and circuit simulations are used to predict $T_{f,\min}$. Because of the voltage variation in $C_d(V)$, $\omega_d(V)$ varies with voltage. We use a large-signal cutoff frequency, $\omega_{d,ls} = 1/R_d C_{ls}$, rather than $\omega_d(0)$ as a standard of comparison between diode designs because stronger correlation between $T_{f,\min}$ and $\omega_{d,ls}$ is seen in circuit simulations. Fig. 3(a) shows a SPICE simulation of shock formation on a 147-section NLTL with $Z_{ls}(0, -6\text{ V}) = Z_{\rm load} = 50\ \Omega$, and $\omega_{\rm per}/2\pi = \omega_{d,ls}/2\pi = 500$ GHz. For a 0 to -6 V, 20 ps $T_{f,\rm in}$ (10%–90%) input, a 2.9 ps fall time output with zero overshoot is generated.

If the Bragg frequency dominates $(\omega_{\rm per} \ll \omega_{d,ls})$, then $T_{f,\min} \propto 1/\omega_{\rm per}$ and shock wavefronts show strong ringing at the Bragg frequency. Fig. 3(b) shows a SPICE simulation of shock formation on a 50-section NLTL with $\Delta T(0\text{ V}, -6\text{ V}) = 50$ ps, $Z_{ls}(0, -6\text{ V}) = Z_{\rm load} = 50\ \Omega$, $\omega_{\rm per}/2\pi = 100$ GHz, and $\omega_{d,ls}/2\pi = 2$ THz. The input fall time is 50 ps and the output has a 2.4 ps fall time and shows strong and sustained ringing. Increasing $\omega_{d,ls}$ relative to $\omega_{\rm per}$ progressively increases both the magnitude and the duration of the shock-wave ringing. With $\omega_{\rm per} \ll \omega_{d,ls}$ and with either impulsive or sinusoidal inputs, trains of solitons are generated [12], [26]. While *impulse* compression on NLTL's has been demonstrated [27], [28] using soliton propagation, the topic is beyond the scope of this text.



(a)

(b)

(c)

Fig. 3. SPICE simulations of fall time compression showing the relative effects of $\omega_{\rm per}$ and $\omega_{d,ls}$: (a) 2.9 ps fall time NLTL shock formation with diode cutoff frequency dominant; $\omega_{\rm per}/2\pi = \omega_{d,ls}/2\pi = 500$ GHz. (b) 2.4 ps fall time NLTL shock formation with Bragg frequency dominant; $\omega_{\rm per}/2\pi = 100$ GHz, $\omega_{d,ls}/2\pi = 2$ THz. (c) 0.9 ps fall time NLTL shock formation with Bragg and diode cutoff frequencies chosen to have comparable effects on compressed fall time. $\omega_{\rm per}/2\pi = 500$ GHz, $\omega_{d,ls}/2\pi = 2$ THz. Partial shock formation is also evident. Voltages are shown at the input, at 15-diode intervals, and at the output.

Circuit simulations indicate that $\omega_{d,ls}$ and $\omega_{\rm per}$ have comparable effects on $T_{f,\min}$ if the diode cutoff frequency is four to six times the Bragg frequency. With $\omega_{d,ls}$ and $\omega_{\rm per}$ in these proportions, shock waves are generated with moderate ringing. Fig. 3(c) shows a SPICE simulation of NLTL shock formation on a 147-section line with $\omega_{\rm per}/2\pi = 500$ GHz, $\omega_{d,ls}/2\pi = 2$ THz, and a 0.9 ps output fall time. The formation and growth of a partial shock wave are also evident.

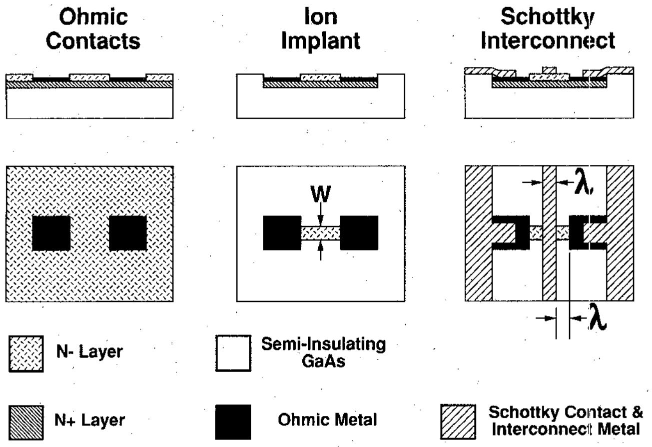


Fig. 4. NLTL fabrication sequence. Ohmic contacts to the N^+ layer are followed by a proton isolation implant and a Ti/Pt/Au lift-off which creates both the Schottky contacts and metal interconnections. λ is the process minimum feature size.

III. Diode Design

For picosecond shock generation, the diodes must have several terahertz cutoff frequencies, strongly varying depletion capacitance, and a breakdown voltage sufficient to support the ~5–10 V shock wave amplitudes. These parameters depend upon the diode doping profile and geometry.

First consider the fabrication sequence (Fig. 4). Starting with a semi-insulating GaAs substrate, a heavily doped N^+ buried layer is grown, which serves as the diode cathode connection. A surface N^- diode active layer, preferably with a hyperabrupt doping profile, is then grown. Ohmic contacts to the N^+ layer are formed by a recess etch through the N^- layer, a self-aligned AuGe/Ni/Au lift-off, and a subsequent anneal. Proton implantation converts the N^+ and N^- layers to semi-insulating material [29], defining diode contact areas and eliminating N^+ and N^- layer conductivities adjacent to transmission lines, which would otherwise cause substrate conductivity losses. The ~1.4 μm maximum proton penetration depth [29] with typical 200 keV ion implanters limits the combined N^+ and N^- layer thicknesses. During implantation the diode regions are protected by a 1–2 μm Au on polyimide mask. Interconnections are formed with a Ti/Pt/Au lift-off; Schottky contacts result where this metal layer overlays the unimplanted N^- layer. Diode contact areas are independent of mask misalignments, and the only critical alignment is the lateral (in the orientation of Fig 4) registration between the ohmic and Schottky masks. Diode minimum dimensions of 2–3 μm are easily attained in processing and are sufficient for $\omega_{d,ls}/2\pi \simeq 2$–4 THz.

Given an exponentially graded hyperabrupt doping profile $N_d^-(x) = N_0 \exp(-x/x_0)$ [8], the diode capacitance is given implicitly by

$$V+\phi = \frac{qN_0x_0^2}{\epsilon}\left(1-\left(1+\frac{\epsilon A}{C_d(V)x_0}\right)e^{-\epsilon A/C_d(V)x_0}\right) \qquad (9)$$

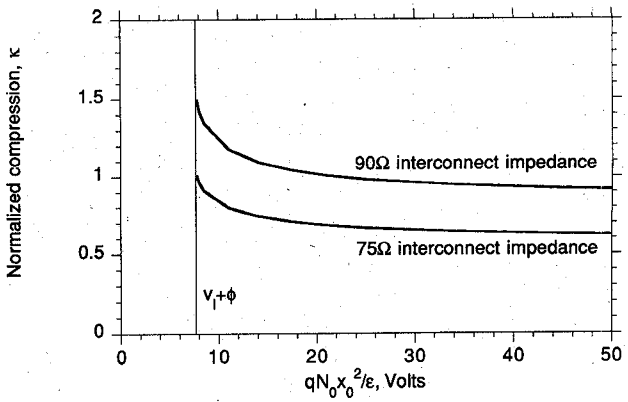


Fig. 5. Normalized NLTL compression κ as a function of diode doping parameters. $Z_{ls} = 50\ \Omega$, $Z_1 = 90\ \Omega$, $V_l = -7$ V.

where $\phi = 0.8$ V, $\epsilon = 13\epsilon_0$ is the GaAs permittivity, and A is the diode junction area.

Combine (1), (4), and (7) to find the NLTL fall time compression ΔT normalized to the propagation delay of the unloaded high-impedance CPW:

$$\begin{aligned}\kappa &= \frac{\Delta T(V_h,V_l)}{\tau} = \frac{v_{\text{cpw}}\,\Delta T(V_h,V_l)}{d}\\ &= \sqrt{1+\zeta C_d(V_h)/C_{ls}(V_l,V_h)}\\ &\quad -\sqrt{1+\zeta C_d(V_l)/C_{ls}(V_l,V_h)} \qquad (10)\end{aligned}$$

where

$$\zeta = \left(\frac{Z_1}{Z_{ls}(V_l,V_h)}\right)^2 - 1 \qquad (11)$$

and $v_{\text{cpw}} = c/\sqrt{7} = 1.13(10^8)$ m/s is the CPW propagation velocity. Since the required NLTL length for shock formation is

$$l \simeq T_{f,\text{in}}d/\Delta T = T_{f,\text{in}}v_{\text{cpw}}/\kappa \qquad (12)$$

κ is maximized to reduce NLTL die area and minimize CPW skin-effect losses. With $V_h = 0$, normalized compression (Fig. 5) is a function of $Z_{ls}/Z_1, V_l$, and the doping-dependent parameter $qN_0x_0^2/\epsilon$ (if $qN_0x_0^2/\epsilon < V_l + \phi$, the diode depletion region extends into the N^+ layer and (9) does not hold). As shown in Fig. 5, diodes with more abrupt doping profiles yield larger compression and therefore reduce the required NLTL length. Reduced die area and reduced skin effect losses are thereby attained. Unfortunately, as the diode doping profile is made more abrupt ($qN_0x_0^2/\epsilon$ decreased) the diode cutoff frequency will also decrease.

Given minimum diode dimensions (process resolution) of λ (Fig. 4), we can calculate $\omega_{d,ls}$. Given $A = w\lambda, C_d(V)$ is calculated from (9). Series resistance includes ohmic contact resistance $R_c = \rho_c/2w$, where ρ_c is the specific contact resistivity. The series resistance of the N^+ layer, including spreading resistance under the Schottky contact, is $R_{N^+} = 7\rho^+\lambda/12wT^+$, where ρ^+ and T^+ are the resistivity and thickness of the N^+ layer. T^+ is limited by the maximum proton implant depth available, while ρ^+ is

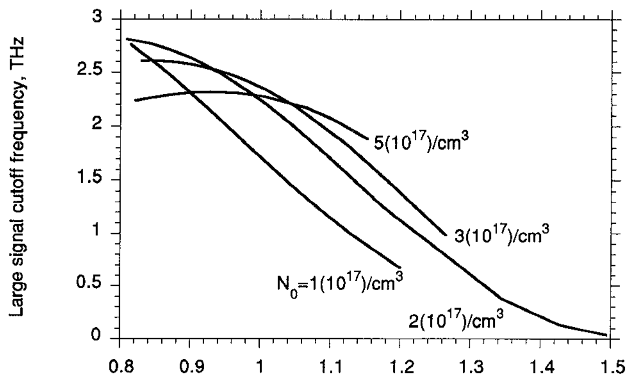


Fig. 6. Large-signal cutoff frequency versus normalized NLTL compression, with surface doping N_0 as a parameter. $\lambda = 3\ \mu$m $Z_{ls} = 50\ \Omega$, $Z_1 = 90\ \Omega$, $V_l = -7$ V.

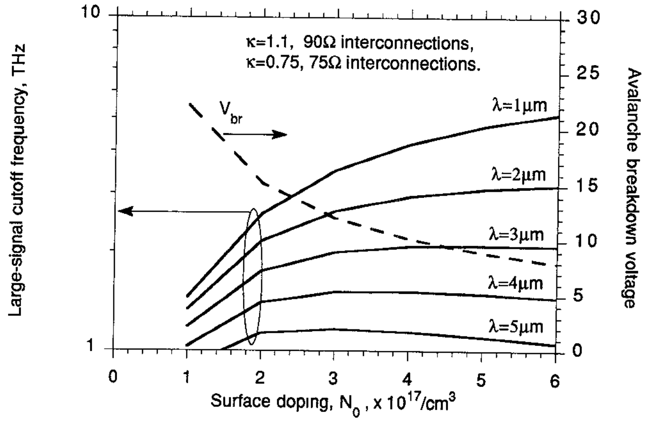


Fig. 7. Large-signal cutoff frequency and approximate breakdown voltage versus surface doping N_0 and process resolution λ. Normalized compression is constant ($qN_0x_0^2/\epsilon = 14.1$ V) at 1.1 for $Z_1/Z_{ls} = 90\ \Omega/50\ \Omega$, 0.75 for $Z_1/Z_{ls} = 75\ \Omega/50\ \Omega$. $V_l = -7$ V.

constrained by doping limits in growth. The portion of the N^+ layer between the bottom of the depletion layer and the N^-–N^+ interface contributes a resistance at zero bias of

$$R_{N^-} = \int_{x_{j0}}^{T^-} \rho_-(N_d^-(x))\,dx = \int_{x_{j0}}^{T^-} \rho_-\left(N_0 e^{-x/x_0}\right) dx \qquad (13)$$

where $\rho_-(N_d^-(x))$ is the doping-dependent N^- resistivity and x_{j0} is the zero-bias depletion depth. R_{N^-} is rapidly reduced as the diode is reverse-biased; since this cannot be modeled in SPICE, circuit simulations pessimistically assume the full zero-bias resistance. To minimize R_{N^-}, the N^- layer thickness, T^-, is set at the diode depletion depth at the maximum negative voltage V_l. In our process, currently $T^+ + T^- = 1.4\ \mu$m, $\rho_c = 20\ \Omega\cdot\mu$m, and $\rho^+ = 7.5\ \Omega\cdot\mu$m ($6\times10^{18}$/cm^3 N^+ doping).

For a given process resolution λ, higher compression results in lower diode cutoff frequency and there is an optimum surface doping dependent upon λ and κ (Fig. 6). For $Z_1/Z_{ls} = 90\ \Omega/50\ \Omega$ normalized compressions of 1–1.1 are attained without large sacrifices in $\omega_{d,ls}$. Fixing $\kappa = 1.1$, Fig. 7 shows $\omega_{d,ls}/2\pi$ versus process resolution. To exploit smaller diode dimensions, surface doping must be increased and (holding κ constant) x_0 and T^- decreased. The avalanche breakdown voltage then decreases (Fig. 7). For N_0 above $\sim 5(10^{17})$/cm^3 tunneling currents become substantial, and the reverse breakdown voltage is then smaller than shown in Fig. 7. Diodes with minimum dimensions of $\lambda = 2$–$3\ \mu$m can attain 10–15 V breakdown voltages and 2–3 THz cutoff frequencies, while maintaining reasonable normalized compression. If the process resolution is improved to $\lambda = 1\ \mu$m, diode cutoff frequencies can be increased to approximately $\omega_{d,ls}/2\pi = 4$–5 THz before the breakdown voltage becomes too small to support 5–7 V shock generation.

IV. NLTL Layout

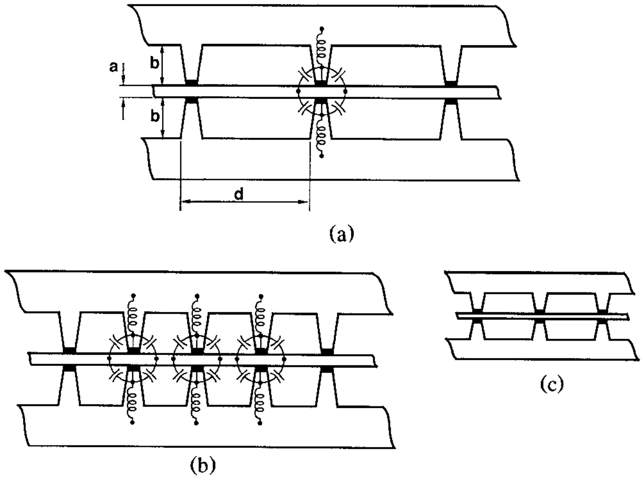


Fig. 8. (a) NLTL cell layout showing interconnection parasitics. (b) Parasitics will dominate if the CPW dimensions a and b are held constant when the Bragg frequency is scaled. (c) To proportionally reduce parasitics while scaling ω_{per}, the CPW dimensions must also be scaled.

Circuit layout introduces parasitic series inductance and shunt capacitance at the diode locations. CPW skin loss is a major parasitic which must be minimized. These factors are interrelated. Microstrip circuits require through-wafer holes (vias) for ground connections having ~ 10 pH inductance ($j18\ \Omega$ at 300 GHz) for a 100-μm-thick substrate. Monolithic NLTL's are thus implemented using CPW lines. The cell layout is shown in Fig. 8. The dimensional ratio (Fig. 8) a/b is set by the CPW characteristic impedance, which on GaAs is

$$Z_1 \approx 11.3\ \Omega \times \ln\left(2\frac{1+\sqrt[4]{1-k^2}}{1-\sqrt[4]{1-k^2}}\right) \qquad (14)$$

for $0 \leqslant k \leqslant 1/\sqrt{2}$, where $k = a/(a+2b)$. The CPW ground plane is extended toward the center conductor to make contact with the diode ohmic contact. Both inductance in series with the diode and capacitance between the CPW center conductor and ground plane extension (fin) are introduced. Neither parasitic is readily calculated, but both increase as the CPW lateral dimensions are increased, and these parasitics will become comparable to the CPW inductance L and capacitance C_l if the diode spacing d is equal to the CPW signal–ground separation b (Fig. 8(b)). We therefore constrain the CPW ground–ground spacing to

$$1.5(a+2b) \leqslant d. \qquad (15)$$

For a required Bragg frequency and Z_{ls}, the diode spacing must be

$$d = v_{\text{cpw}}\tau = v_{\text{cpw}} \times \frac{2Z_{ls}}{Z_1\omega_{\text{per}}} \qquad (16)$$

(where $v_{\text{cpw}} = 1.13(10^8)$ m/s), while the diode junction area must be chosen to give a large-signal capacitance of

$$C_{ls} = \frac{2}{Z_{ls}\omega_{\text{per}}}\left(1 - \frac{Z_{ls}^2}{Z_1^2}\right). \qquad (17)$$

Small $T_{f,\min}$ requires high ω_{per} and hence small d. The CPW ground–signal separation b then becomes small, as does (with fixed Z_1, eq. (14)) the center conductor width a.

The NLTL small-signal attenuation arises from diode resistance and skin-effect losses, the latter increasing as $1/a$. With n sections the attenuation is [8]

$$S_{21}(\omega, V) = \exp\left[-n\omega^2 C_d^2(V) R_d Z_0(V)/2 - r_l/2Z_0(V)\right] \qquad (18)$$

where r_l is the center conductor skin resistance

$$R_l = \max\begin{cases} \rho l/at \\ (l/a)\times\sqrt{\omega\mu/2\sigma} \end{cases} \qquad (19)$$

t is the metal thickness, and the total NLTL length, $l = nd$, is given by (12). The high Bragg frequencies required for small $T_{f,\min}$ force narrow CPW dimensions and high CPW losses. The losses not only decrease output amplitude but also increase output fall time because the reduced signal swing reduces the fractional variation in diode capacitance.

The wavefront fall time decreases with distance (Fig. 3); hence high ω_{per} is required only near the NLTL output, where the transition times are short. To minimize losses while attaining short fall time, we use low-loss NLTL cells with low ω_{per} near the input and higher loss (high ω_{per}) cells with a small $T_{f,\min}$ near the line output. An NLTL using two cascaded sections [17], [8] with low and high ω_{per} attains lower losses than untapered structures. Because the compressed fall time approaches $T_{f,\min}$ ($T_{f,\min} \propto 1/\omega_{\text{per}}$), significant ringing (Fig. 9(a)) is generated in the first line section with low ω_{per}. The second line section has smaller $T_{f,\min}$, thereby further compressing the shock fall time, but the ringing generated from the first line section is not suppressed. For picosecond instrumentation, minimum ringing is desired. Ringing can be reduced by varying the diode spacing, as suggested in private communications by J. Goll (Tektronix). In an exponentially tapered NLTL the Bragg frequency at the nth NLTL section $\omega_{\text{per},n} = k\omega_{\text{per},n-1} (k > 1)$ increases continuously with distance. The local Bragg frequency is kept much larger than the inverse of the wavefront fall time at that point, and overshoot and oscillation are greatly suppressed (Fig. 9(b)).

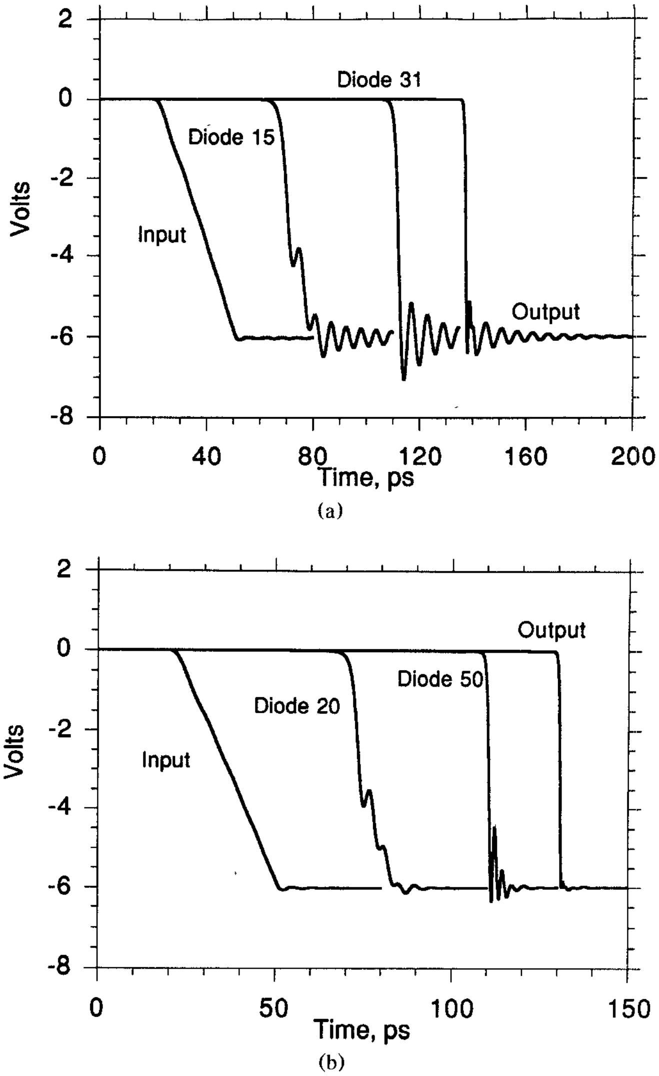


Fig. 9. SPICE simulations comparing step-tapered and exponentially tapered NLTL's. (a) Shock formation on a step-tapered NLTL with 50 ps compression and having 30 sections with $\omega_{\text{per}} = 125$ GHz and 40 sections with $\omega_{\text{per}} = 500$ GHz. Ringing generated by the first line section (diode 31) propagates to the line output. 25 ps input and 0.9 ps output fall time. (b) SPICE simulation of shock formation on an exponentially tapered NLTL with 50 ps compression and with ω_{per} grading from 125 GHz at the input to 900 GHz at the output. The 0.7 ps fall time output shows only small oscillation.

With fixed input fall time, $T_{f,\text{in}}$, increasing the interconnect impedance Z_1 increases the normalized compression (eq. (10)) and hence reduces the required NLTL length (eq. (12)), but the higher impedance results in narrower CPW conductor widths a (eqs. (14) and (15)). Total NLTL skin loss is proportional to the sum $\Sigma(d/a)$ over the NLTL length, and loss is minimized given the appropriate choice of interconnect impedance Z_1 (Fig. 10). Z_1 of approximately 75 Ω maintains low skin losses and short NLTL length.

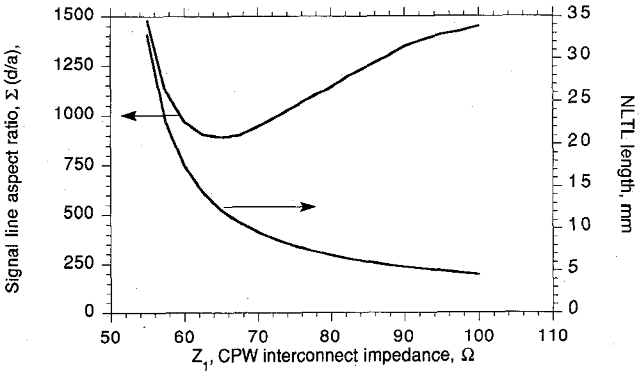


Fig. 10. Minimizing NLTL loss: NLTL length and number of squares of metal (length/width aspect ratio) of the CPW center conductor, as a function of Z_1 for an exponentially tapered NLTL as in Fig. 9. The NLTL has 50 ps compression, $Z_{ls} = 50\ \Omega$, $V_h = 0$ V and $V_l = -7$ V, and the diode doping parameter is $qN_0x_0^2/\epsilon = 14.1$ V.

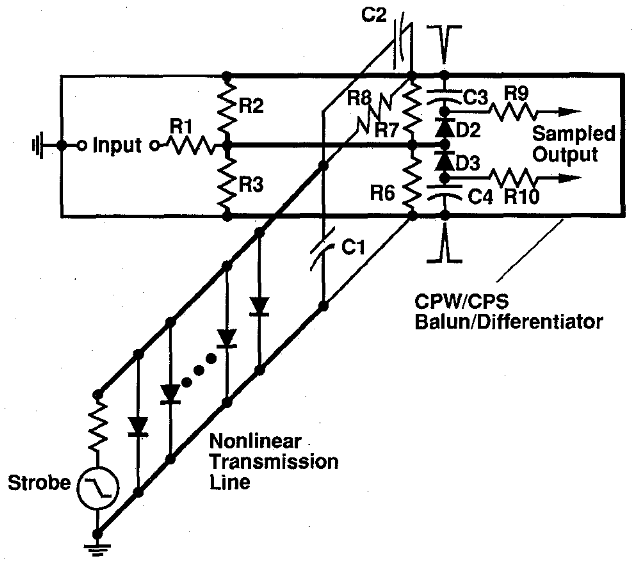


Fig. 11. Sampling circuit schematic diagram.

V. MILLIMETER-WAVE SAMPLING CIRCUITS

Sampling circuits as used in microwave sampling oscilloscopes [3], network analyzers, counters [5], and frequency synthesizers (as sampling phase detectors [6]) are both the primary application for the NLTL [19]–[21] and the best tool for NLTL characterization.

A. Design Considerations

A sampling circuit consists of a strobe pulse generator, a diode/resistor bridge, and a balun/differentiator. In addition to the NLTL requirements of diodes and line sections, direct implementation of a sampling circuit requires process steps for coupling and hold capacitor fabrication and air bridges for interconnections. With appropriate circuit layout, these additional process steps can be eliminated, allowing simple fabrication of monolithic sampling circuits. The circuit diagram is shown in Fig. 11 and its layout in Fig. 12.

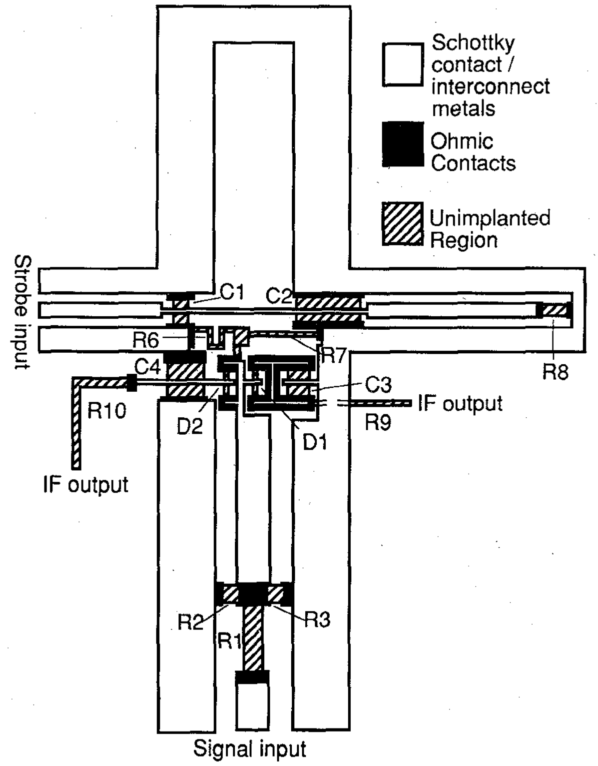


Fig. 12. Sampling circuit layout.

In the circuit (Fig. 11) an NLTL (using the design of Fig. 9(b)) compresses an input strobe signal, either a step function or a microwave sine wave (10%–90% fall time = $0.3/f_{\text{in}}$). The sampling diodes must be gated by a pair of symmetric positive and negative impulses. These are generated from the NLTL output using a balun/differentiator network implemented using the coplanar strip (CPS) mode of the input signal coplanar waveguide (CPW). Coupled through the network R_8, C_1, and C_2, the strobe step function is applied between the CPW ground planes, and propagates on them in both directions as a CPS mode. At a distance d_{short} from the sampling diodes, a short circuit (on the left) and R_2 and R_3 (on the right) reflect the CPS mode, generating an impulse at the sampling diodes of duration equal to the $2d_{\text{short}}/v_{\text{cpw}}$ round-trip delay.

The sampling diodes (D_2 and D_3) are held in reverse bias by two high-impedance supplies connected through R_9 and R_{10}. The complementary strobe pulses are coupled through the large capacitors C_3 and C_4 and applied across the sampling diodes, which are then driven into forward conduction for a period comparable to the duration of the strobe impulse. During this period, the sampling aperture time, the input (RF) signal partially charges the coupling capacitors. If the repetition frequency of the RF input signal is a multiple nf_0 of the strobe frequency (local oscillator, or LO), at each successive strobe interval the sampling diodes will further charge the coupling capacitors C_1 and C_2, and the common-mode (average) voltage of the two sampled outputs (coupled through RF isolation resistors R_9 and R_{10}) will asymptotically approach the RF input voltage. The repetition frequency of the RF input signal is then offset in frequency by Δf from a multiple nf_0 of the strobe frequency f_0, and the sampling signal is then mapped out in equivalent time at a repetition frequency of Δf.

To simplify processing, the sampling coupling and compensation capacitors $C_1 - C_4$ can be replaced with reverse-biased diodes. Air bridge wiring crossovers can be eliminated by using diode N^+ buried layers. Where crossed by the strobe line, the buried N^+ layers of compensation capacitors C_1 and C_2 provide continuity for the input signal CPW ground planes. The N^+ layer of coupling capacitor C_4 connects the input signal CPW ground planes where they are crossed by the first sampled signal (IF) output, and the second IF output crosses beneath the CPW ground plane using the N^+ layer of C_3. The maximum linear input voltage is small; hence a 20:1 input attenuator (R_1, R_2, and R_3) is used to allow testing NLTL output signals of ~ 5 V. R_2 and R_3 of the sampler input attenuator short the CPW ground planes, eliminating the need for an air bridge at that position.

Since RF input voltages greater than the sampling diode reverse bias will inadvertently forward bias the sampling diodes, V_{bias} sets the maximum input voltage. To ensure diode conduction during the sampling interval, V_{bias} must also be less than the strobe impulse magnitude developed at the sampling diodes. Hence, the sampling circuit dynamic range is set by the NLTL strobe pulse amplitude and the differentiator efficiency. Attained NLTL output voltages are $\sim 2:1$ smaller than the strobe amplitudes used in SRD-gated sampling circuits, and the differentiator/balun must therefore have high efficiency. Without the matching and compensation capacitors C_1 and C_2, the peak stobe impulse magnitude is a fraction of the NLTL output voltage, through voltage division between the $R_8 = 50\ \Omega$ NLTL termination resistor and the parallel impedances $Z_{\text{CPS}}/2 = 50\ \Omega$ of the counterpropagating CPS modes. The strobe impulse is further attenuated through the parasitics of the sampling diodes. Adding capacitors C_1 and C_2, a $C-L-C$ π-section matching network is formed from the two capacitors, the shorted CPS line inductance, and the termination resistor R_8. Nearly the full NLTL output voltage can be developed across the sampling diodes while maintaining a low reflection termination to the NLTL.

The sampling circuit rise time (hence bandwidth) is determined by the signal line RC time constant and by the aperture time. The two sampling diode capacitances load the RF line, thus introducing a 10%–90% rise time contribution of $2.2(Z_0/2)2C_{\text{diode}}(V_{\text{bias}})$, where $Z_0 = 50\ \Omega$ and $C_{\text{diode}}(V_{\text{bias}})$ is the sampling diode capacitance. Aperture time is determined by the NLTL-generated strobe fall time, by the round-trip delay of the shorted-line differentiating network, by broadening of the differentiated strobe pulse by the sampling diode capacitance, and by the diode reverse bias V_{bias} relative to the impulse peak voltage. The round-trip time of the CPS shorted line differentiator should be approximately equal to the NLTL fall time. Larger round-trip times broaden the strobe impulse while shorter round-trip times reduce the impulse amplitude without significant reduction in the impulse duration. In the absence of sampling diode parasitics, the strobe (full width at half maximum) impulse duration is then the NLTL output fall time. The diode capacitances and series resistances further broaden the strobe impulse at the sampling diodes. With given strobe impulse duration, increasing the diode reverse bias decreases the duration of forward conduction, and with reverse bias approaching the strobe peak amplitude, the aperture time can be reduced to a fraction of the strobe impulse duration (hence strobe NLTL fall time). Monolithic fabrication permits ~ 3–10 fF sampling diode capacitances, yielding subpicosecond signal line RC time constants, while a monolithic NLTL strobe generator permits picosecond aperture times.

B. NLTL and Sampling Circuit Results

Picosecond pulse generators require picosecond instruments for their characterization. To evaluate the rise time of our circuits, the output of an NLTL pulse generator is connected to an on-wafer NLTL-gated sampling circuit. In this manner, we measure the combined (convolved) responses of sampling circuit and NLTL shock-wave generator. The experimental results of NLTL and sampling circuit are inseparable.

NLTL's were fabricated using $\lambda = 3\ \mu$m design rules on semi-insulating GaAs material with a 1-μm-thick $6(10^{18})/\text{cm}^3$ doping N^+ layer, and an N^- layer with $N_0 = 2(10^{17})/\text{cm}^3$, $x_0 = 225$ nm, and $T^- = 425$ nm. These parameters are not optimum for cutoff frequency ($\omega_{d,ls}/2\pi = 1.7$ THz, Fig. 7), but were chosen to maintain moderate breakdown voltage (15 V, predicted, Fig. 7, versus 12.5 V measured) required for other (soliton compression [27]) circuits on the wafer. The exponentially tapered NLTL design of Fig. 9(b) was used (125 GHz input and 900 GHz output Bragg frequencies, $\Delta T = 50$ ps, 0.7 ps simulated $T_{f,\min}$, 5.5 mm length, $Z_1 = 90\ \Omega$).

Small-signal microwave scattering parameter measurements of the NLTL are useful predictive tools of performance of the NLTL in wavefront compression. Circuit element values are also determined by fitting the measured parameters to the calculated S parameters of the NLTL circuit model. The NLTL group delay (Fig. 13) is nearly independent of frequency, and shows the expected strong variation with voltage. The change in group delay over the 0–6 V range indicates 47 ps compression, hence a measured normalized compression of $\kappa = 1.0$, 10% lower than the design value. The measured small-signal insertion loss is shown in Fig. 14; at the designed 10 GHz input and -3 V bias the attenuation is a significant 4 dB. From the variation of the attenuation with frequency and bias voltage the transmission-line skin-effect losses and the diode series resistance can be determined (eq. (18)). From the measured NLTL input match, S_{11} (Fig. 15), the voltage-dependent characteristic impedance is determined:

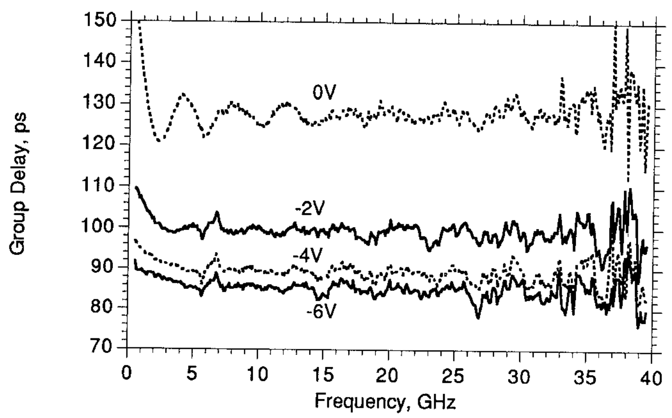


Fig. 13. Small-signal NLTL group delay versus bias and frequency, determined by 45 MHz–40 GHz network analysis.

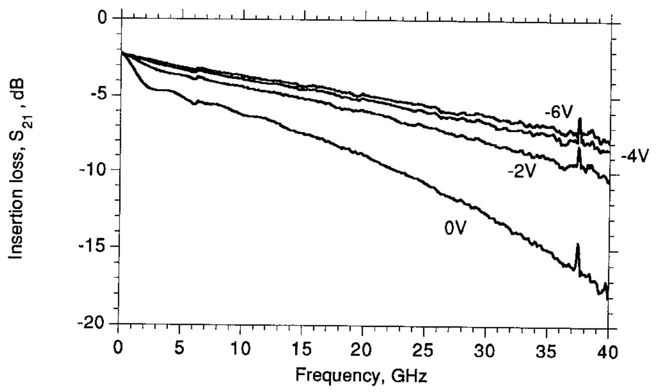


Fig. 14. Small-signal NLTL attenuation versus bias and frequency.

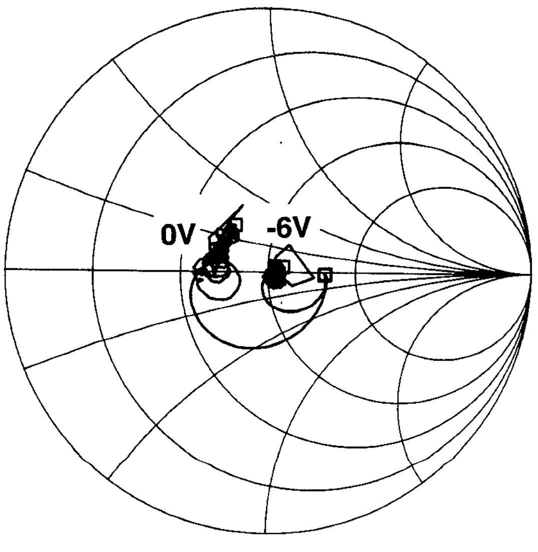
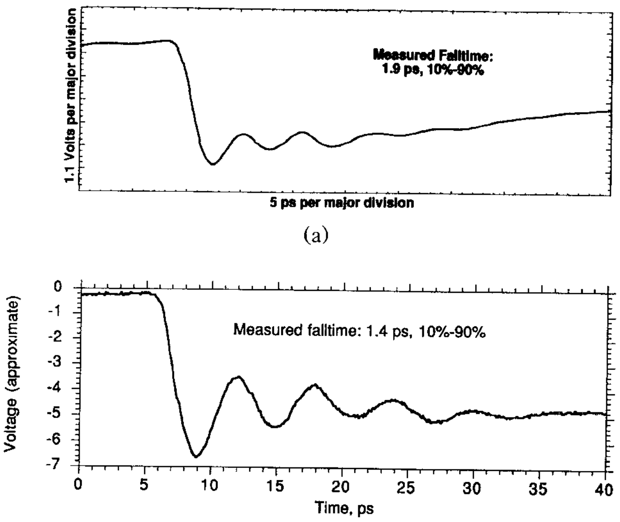


Fig. 15. 45 MHz–40 GHz NLTL input match (S_{11}) at 0 and 6 V reverse bias.

$\simeq 35\ \Omega$ at 0 V bias, and $\simeq 55\ \Omega$ at -6 V. The large-signal characteristic impedance lies between these two extreme values, and is approximately 40–45 Ω, lower than the intended 50 Ω. The NLTL input reflection coefficient (Fig. 15) is much smaller than that of step-recovery diode pulse generators.



(a)

(b)

Fig. 16. NLTL pulse output measured by sampling circuits. (a) Results for a wafer with uniform doping. (b) Results for a wafer with hyperabrupt doping. Substantial ringing occurs with the hyperabrupt wafer because of repeated reflections on a misterminated transmission line section.

Sampling circuits were fabricated on the same wafer using an NLTL strobe pulse generator. A second NLTL provides a test signal input so that the combined fall time (rise time) of the NLTL and sampling circuit can be measured. The 3 μm by 3 μm sampling diodes have a 7.5 fF capacitance, introducing a 0.8 ps signal line RC rise time. With the diodes biased to maintain 1 mA peak impulse current, SPICE simulations predict an aperture time of 0.85 ps with a 1 V reverse sampling diode bias. The predicted 10%–90% fall time (or rise time) of the sampling circuit is then $T_{\text{sampler}} = \sqrt{0.8^2 + 0.85^2} = 1.17$ ps, corresponding to 300 GHz -3 dB calculated bandwidth. In testing, synchronized microwave synthesizers drive the strobe NLTL and the test signal NLTL offset in frequency to yield a 60 Hz IF output frequency. The measured response is the NLTL output waveform convolved with the sampling circuit impulse response.

Owing to MBE growth difficulties, the N^- doping on the first wafer processed was $2(10^{17})/\text{cm}^3$ with negligible grading [20]. At 9 GHz LO drive frequency, the measured (convolved) response of the NLTL and sampling circuit shows 1.9 ps 10%–90% fall time (Fig. 16(a)) [20]. As a result of the exponentially tapered NLTL design, the observed combined step response of the NLTL and sampling circuit is very clean, showing only 24% peak–peak ringing at 167 GHz. Fig. 16(b) shows measured results for a more recent NLTL and sampling circuit, fabricated on MBE material having the designed hyperabrupt profile. The circuit is operated at 7 GHz LO drive frequency and 23 dBm NLTL drive power. The 10%–90% measured fall time of the convolved response is 1.4 ps, approximately 35% shorter than that observed for the uniformly doped wafer. The measured step response shows substantial 167 GHz ringing (6 ps period). In this process run, termination resistors R_6 and R_7 (Fig. 11) were much higher than the intended 100 Ω (i.e., 50 Ω for R_6 and R_7 in parallel). Round-trip reflections then result in the 170-μm-long (3 ps round-trip time) CPW connection between resistors (R_2, R_3) and (R_7, R_8) within the sampling circuit. The numerical Fourier transform of Fig. 16(b) yields a -3 dB bandwidth of 215 GHz for the *combined* response. To verify that the sampling circuit is operating within its linear dynamic range during the rise time measurements, identical sampling circuits with bond-pad inputs were also tested under the same bias conditions with a 7 GHz microwave sinusoidal input of larger amplitude than the NLTL output. No distortion was observed.

The bandwidth and rise time of the sampling circuit and NLTL cannot be uniquely determined from these data. The 1.4 ps 10%–90% measured fall time is consistent with a rudimentary sum-of-squares convolution of the predicted 0.7 ps NLTL and 1.17 ps sampling circuit fall times, which leads to a predicted ~ 300 GHz sampling circuit bandwidth. We estimate a sampling circuit bandwidth between 250 and 300 GHz.

VI. CONCLUSIONS

Owing to limitations in pulse generation technology, the bandwidth of microwave instruments has not kept pace with advances in millimeter-wave transistors and integrated circuits. Based on terahertz diode technology, the NLTL has generated $\leqslant 1.4$ ps step functions and has allowed the development of sampling circuits with ~ 300 GHz bandwidths. Compared with previous technologies, the NLTL and NLTL-based sampling circuits have unprecedented bandwidth, require a die area (6 mm × 1 mm) typical of other GaAs microwave integrated circuits, and require only a simple fabrication process. Commercial sampling oscilloscopes using NLTL strobe pulse generators have recently become available [30]. Using the NLTL, 300 GHz instrumentation for millimeter-wave systems can be developed.

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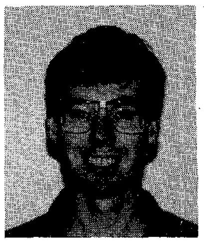

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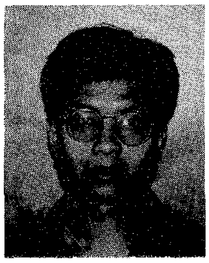

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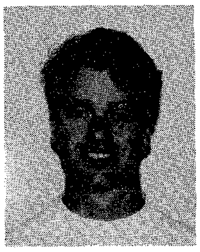

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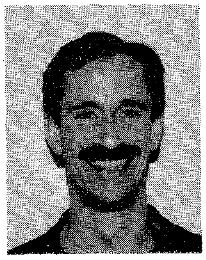

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